EE/CprE/SE 492 BIWEEKLY REPORT 3

Date: ***September 28th, 2023 – October 11th***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Biweekly Summary

Over the course of these past two weeks, there has been a lot of progress on our project. We were able to successfully complete the documentation for the open-source analog design flow. This document turned out to be much longer and more detailed than originally planned. This document is over 12,000 words and 60 plus pages long. As there is no centralized documentation, we decided it would be best to fully detail the entire process from start to finish. This includes environment setup, tool installation, tool configuration, tool usage, and how to push a design through the analog design flow. We hope this document will prove to be useful not only to people at Iowa State - whether it be future senior design teams or people interested in analog chip fabrication - but also to people in the open-source community.

Outside of the documentation, we also continued to make progress in pushing our designs through the analog design flow. We are almost done with both our 1-bit and 3-bit ADCs. We have also made progress on the trans-impedance amplifier. We also recreated our inverter in the correct PDK variation as before it was in the sky130A variation, which does not support ReRAM.

Finally, we also realized that some of the assumptions we made about the Caravel harness were wrong, and we had to slightly change our design to accommodate this. By realizing we made a mistake in our assumptions, we were able to come up with a better circuit schematic and have planned for how we will implement the majority of the logic required for

the ReRAM crossbar compute device. We also came up with a breakdown of work for all of our devices and hope to have all of them fully pushed through the analog design flow by the end of October. We are doing this so we can focus on top-level integration in November.

Past Weeks Accomplishments

- Joshua Thater
    - Finished writing up the documentation for the analog design flow. This is a very lengthy document, but it will be very useful for people new to this process and will walk them through every step of the process.
        - LINK: https://docs.google.com/document/d/1_0DEhFueN_hLGfPhPGRAFyuIDSJiAyLrGLW8UWXjbXk/edit?usp=sharing
    - Redid circuit schematic after realizing our assumptions were wrong.
    - Recreated inverter in correct process variation and pushed it entirely through the analog design flow.
- Aiden Petersen
    - Got simulations running on the digital framework.
    - Fixed syntax and functional errors on ReRAM crossbar behavioral model.
- Matt Ottersen
    - Created Testbench and general design for Transimpedance Amplifier(TIA)
    - Worked on layout for 1-bit ADC
- Regassa Dukele
    - Design and implement the layout for an Opamp
    - Continue working on the layout of a 3-bit ADC

Pending Issues

- Creating a layout of ReRAM device that passes both DRC and LVS checks.
- Need to figure out how to integrate our designs with the harness through Efabless.
- Coming up with the last bit of circuit logic required for the crossbar compute.
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Individual Contributions

Team Member	Individual Contributions	BIweekly Hours	Total Hours
Joshua Thater	Wrote up and finished documentation. Recreated inverter in correct process variation.	26	111

Aiden Petersen	Finished behavioral digital behavioral model and verified it	6	80
Matt Ottersen	Worked on TIA and 1-bit ADC	9	83
Regassa Dukele	Created the layout for the opamp	10	88

Plans for the Upcoming Weeks

- Joshua Thater
    - Create buffer, transmission gate, 2-1 MUX, and 4-1 MUX, and push all of them through the entire analog design flow.
    - Figure out how to create ReRAM and 1T1R layout that passes LVS.
- Aiden Petersen
    - Complete integration and pre-check of a simple inverter design in the digital framework.
- Matt Ottersen
    - Figure out the issue that is occurring when importing spice netlist to create 1 bit ADC
    - Create Voltage Dividers and start working on designs for other necessary components
- Regassa Dukele
    - Continue working on the layout of a 3-bit ADC.
    - Perform a simulation post layout for both ADC and Opamp